## Amendments To the Claims

- 1. (Original) An integrated circuit comprising:
- a power output stage having an output node;
- a controller circuit coupled to the power output stage, the controller circuit to selectively switch the power output stage into a current ramp down mode based on detection of a voltage surge at the output node, the power output stage having an associated current ramp down rate; and
- a processor coupled to the output node and a surge notification input of the power output stage, the power output stage to accelerate the current ramp down rate based on a notification signal from the processor.
- (Original) The integrated circuit of claim 1 wherein the power output stage includes:
- a transistor stack coupled to the controller circuit and having a switching node;
- an output inductor having a first terminal coupled to the switching node of the transistor stack and a second terminal coupled to the output node, the output inductor defining a ramp down current path of the power output stage; and
- a transient adjustment circuit coupled to the output node and a surge notification output of the processor, the transient adjustment circuit to reduce an effective inductance of the ramp down current path in response to the notification signal.
- 3. (Original) The integrated circuit of claim 2 wherein the transient adjustment circuit includes:
  - a surge inductor having a first terminal coupled to the output node; and
- a surge transistor coupled to a second terminal of the surge inductor and the surge notification output, the surge transistor to switch the surge inductor into a parallel connection with the output inductor in response to the notification signal.
- (Original) The integrated circuit of claim 3 wherein the surge notification output is coupled to the surge transistor through a buffer.

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 (Original) The integrated circuit of claim 2 wherein the second terminal of the output inductor is coupled to the output node through a sensing resistor.

- (Original) The integrated circuit of claim 1 wherein the current ramp down mode is to correspond to a gating off of unused portions of the processor.
- (Original) The integrated circuit of claim 1 wherein the notification signal is a pulse signal.
- 8. (Original) The integrated circuit of claim 7 further including a one shot timer coupled to the power output stage and the processor, the one shot timer to receive a level signal from the processor and convert the level signal into the pulse signal based on a ramp down current measurement.
- 9. (Original) The integrated circuit of claim 1 wherein the power output stage is to be coupled to a system voltage and the output node is to be coupled to a processor voltage, the system voltage to be greater than the processor voltage relative to a ground.
- (Original) The integrated circuit of claim 1 further including an output capacitor having a terminal coupled to the output node.
- (Original) The integrated circuit of claim 1 wherein the controller circuit is to switch the power output stage into a current ramp up mode based on a voltage droop at the output node.
- (Original) The integrated circuit of claim 11 wherein the current ramp up mode is to correspond to a gating on of unused portions of the processor.
- (Original) The integrated circuit of claim 11 wherein the controller circuit includes:

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a metal oxide semiconductor field effect transistor (MOSFET) driver coupled to the power output stage;

- a comparator having a first input coupled to the output node and a comparator output coupled to the MOSFET driver; and
  - a reference component to apply a reference voltage to a second input of the comparator.
- (Original) The integrated circuit of claim 13 wherein the reference voltage component is a Zener diode.

## 15. (Original) A computer system comprising:

a power supply; and

an integrated circuit, the integrated circuit including a power output stage, a controller circuit coupled to the power output stage, and a processor coupled to a surge notification input of the power output stage, the power output stage to receive a system voltage of the power supply and having an output node to receive a processor voltage of the power supply, the controller circuit to selectively switch the power output stage into a current ramp down mode based on a voltage surge at the output node, the power output stage having an associated current ramp down rate, the power output stage to accelerate the current ramp down rate based on a notification signal from the processor.

- 16. (Original) The computer system of claim 15 wherein the power output stage includes:
  - a transistor stack coupled to the controller circuit and having a switching node;
- an output inductor having a first terminal coupled to the switching node of the transistor stack and a second terminal coupled to the output node, the output inductor defining a ramp down current path of the power output stage;
- a transient adjustment circuit coupled to the output node, a ground of the power supply and a surge notification output of the processor, the transient adjustment circuit to reduce an effective inductance of the ramp down current path in response to the notification signal.

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17. (Previously Presented) The computer system of claim 16 wherein the transient adjustment circuit includes:

- a surge inductor having a first terminal coupled to the output node; and
- a surge transistor coupled to a second terminal of the surge inductor and the surge notification output, the surge transistor to switch the surge inductor into a parallel connection with the output inductor in response to the notification signal.
- (Original) The computer system of claim 17 wherein the surge notification output is coupled to the surge transistor through a buffer.
- (Original) The computer system of claim 16 wherein the second terminal of the output inductor is coupled to the output node through a sensing resistor.
- (Original) The computer system of claim 15 wherein the current ramp down mode is to correspond to a gating off of unused portions of the processor.
- (Original) The computer system of claim 15 wherein the notification signal is a pulse signal.
  - 22. (Canceled)
  - (Canceled)
  - (Canceled)
  - 25. (Canceled)
  - 26. (Canceled)
  - 27. (Previously Presented) An integrated circuit comprising:

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a power output stage, the power output stage including a transistor stack, an output inductor and a transient adjustment circuit, the transistor stack having a switching node, the output inductor defining a ramp down current path and having a first terminal coupled to the switching node and a second terminal coupled to an output node of the power output stage;

- a controller circuit coupled to the power output stage, the controller circuit including a metal oxide semiconductor field effect transistor (MOSFET) driver, a comparator and a reference component, the MOSFET driver coupled to the transistor stack of the power output stage, the comparator having a first input coupled to the output node and a comparator output coupled to the MOSFET driver, the reference component to apply a reference voltage to a second input of the comparator; and
- a processor coupled to the output node and having a surge notification output coupled to a surge notification input of the transient adjustment circuit, the transient adjustment circuit to reduce an effective inductance of the ramp down current path in response to a surge notification signal from the processor, the notification signal to correspond to a gating off of unused portions of the processor.
- (Original) The integrated circuit of claim 27 wherein the transient adjustment circuit includes:
  - a surge inductor having a first terminal coupled to the output node; and
- a surge transistor coupled to a second terminal of the surge inductor and the surge notification output, the surge transistor to switch the surge inductor into a parallel connection with the output inductor in response to the notification signal.
- (Original) The integrated circuit of claim 28 wherein the surge notification output is coupled to the surge transistor through a buffer.
- 30. (Original) The integrated circuit of claim 27 further including an output capacitor having a terminal coupled to the output node.

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